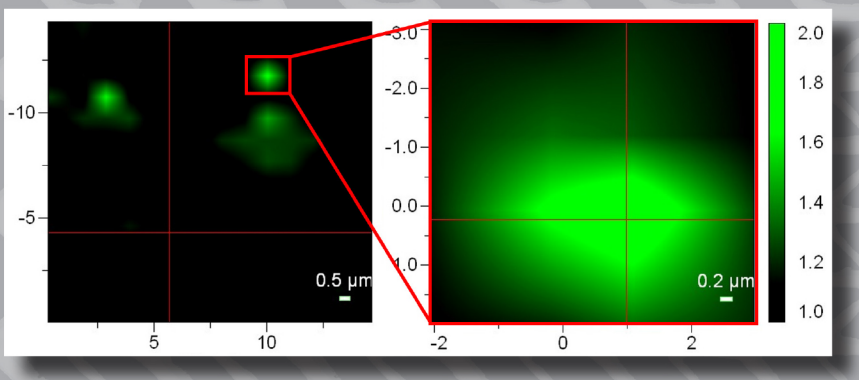
Advancing Silicon Carbide Electronics Technology I

Metal Contacts to Silicon Carbide: Physics, Technology, Applications



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Edited by

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Cover illustration:

Spatial distribution of sub-micron Ni_2Si inclusions in a NiSi Schottky contact formed on 4*H*-SiC. The images were obtained by two-dimensional micro-Raman mapping Ni_2Si band (140 cm^{-1}) intensity normalized to the signal background. See Chapter 3 in this volume for the in-depth review of inhomogeneous SiC Schottky contacts characterisation.

The figure is taken (with minor editing) from I. Nikitina, K. Vassilevski, A. Horsfall, N. Wright, A.G. O'Neill, S.K. Ray, K. Zekentes, and C.M. Johnson, "Phase composition and electrical characteristics of nickel silicide Schottky contacts formed on 4*H*-SiC," *Semiconductor Science and Technology*, vol. 24, no. 5, pp. 055006, 2009. doi:10.1088/0268-1242/24/5/055006

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Table of Contents

Preface

Silicon carbide is a wide band gap semiconductor material possessing unique physical, chemical and electrical properties. Its high critical electric field and thermal conductivity make silicon carbide an excellent material for fabrication of high-power, low-loss semiconductor devices. High thermal stability, outstanding chemical inertness and hardness potentially allow SiC devices to operate in harsh environment at high-temperature conditions. Silicon carbide electronics has a rich history starting from carborundum detectors, the first commercial semiconductor devices released in 1906 [1] but shortly replaced by vacuum tubes. Development of a new growth method to produce high quality SiC crystals in the middle 50^{th} [2] resulted in the resurrection of silicon carbide as a material for the semiconductor electronics. The start of this period was marked by the first silicon carbide conference in Boston in 1959 [3]. In the following two decades, extensive study of SiC material properties was performed and SiC processing technology was significantly improved but availability only of irregular shaped SiC platelets allowed just small scale production of blue and yellow SiC LEDs for specific applications. Seeded growth of SiC crystals was invented in the late 70th [4] and paved the way to large scale manufacturing of SiC devices. Development of SiC epitaxy in the late 80th [5] and introduction of standard size SiC wafers and blue LEDs to the market in the early 90th resulted in the renaissance of the interest to SiC as a material for commercial electronics.

Although SiC LEDs were replaced in the market by more efficient III-N LEDs in the end 90th, developed SiC growth and processing technology was not vanished. Rapid growth of using renewable energy and introduction of strict measures to reduce the carbon footprint in the last decade resulted in a great demand for highly efficient power electronics. Silicon carbide with its outstanding properties and developed growth and processing technology became a material of choice for a new generation of semiconductor power devices. Today, SiC Schottky diodes and MOSFETs are commercially available on the market and silicon carbide electronics is recognized as an essential part of modern industry occupying its own niche of highly efficient power semiconductor devices. This results in a remarkable intensification of research in SiC technology stimulated by growing demand for improving performance and reliability of SiC devices and cost efficiency of their commercial production. An additional driving force of further development of SiC technology is a great potential of silicon carbide as a material for high temperature and high frequency electronics, which is still not realized and awaiting for convincing demonstration of SiC advantageous over conventional semiconductors for these applications.

Since 1993, the progress and latest trends in the field are regular discussed at International and European Conferences on Silicon Carbide and Related Materials. Now, proceedings of these conferences are published every year and widely disseminated. At the same time, detailed reviews and in-depth analysis of current state in SiC material characterization, crystal growth and device processing technology are given in the series of hardcover books. The first book of this kind was published in 1997 [6]. It was edited by Wolfgang J. Choyke, Hiroyuki Matsunami and Gerhard Pensl who collected about 50 papers covering the whole field from SiC fundamental properties, crystal growth and material characterization through to device processing and to the design and applications of SiC devices. It was very popular in scientific community for many years and even nicknamed as a “blue book“. In 2004, it received an update with the most recent developments in SiC electronics [7] and remains very relevant as an essential reference book up to now. Few more edited books were published [8-15] from that time till 2015. They provided collections of review papers in various subjects of SiC electronics selected according to editors preferences. In 2014, a classical textbook was published by Tsunenobu Kimoto and James A. Cooper [16]. In contrast to other books, it does not aim to give a complete in-depth overview of each topic but seamlessly describes silicon carbide technology from material properties to system applications of SiC devices. These are all the books published on SiC in 21st century to the best of our knowledge and we believe that a new book is right on-time to support the periodicity of publications and to review the state-of-the art in rapidly advancing SiC technology.

SiC science and technology became matured during two last decades and include many aspects from basic physics to electrical circuit design. Obviously, all of them can be barely covered in a single volume. Bearing this in mind, we limited the scope of our book mainly by SiC device processing technology. The first volume of this book is devoted to an important part of SiC device processing which is fabrication and characterization of metal contacts. The volume is opened with Chapter 1 focusing on silicon carbide surface cleaning which is the first and essential step in any device processing. It is followed by Chapter 2 describing fundamental physics, electrical characterization methods and processing of ohmic contacts to silicon carbide. The chapter provides detailed analysis of contact resistivity dependence on material properties, limitations and accuracy of contact resistivity measurements, practical advises on ohmic contact fabrication and test structure design, critical overview of different metallization schemes and processing technologies reported up to now. Thermal stability of ohmic contacts to SiC, their protection and compatibility with device processing are also discussed in this chapter. In Chapter 3, the basic physical

principles of Schottky barrier formation are recalled and adapted to the specific case of SiC. Next, the important fundamental topic of Schottky barrier inhomogeneity in SiC materials is introduced. Then, a section of this chapter is devoted to the technology and design of 4H-SiC Schottky and Junction Barrier Schottky diodes. Si/SiC heterojunction diodes are also briefly discussed in this chapter as a particular case of rectifying contacts. Some common applications of SiC Schottky diodes in power electronics and temperature/light sensors are provided in the last section of this chapter. The volume is concluded with Chapter 4 reviewing high power SiC unipolar and bipolar switching devices. The challenges and prospects of different types of SiC devices including material and technology constraints on the device performance are discussed in this chapter to elucidate the main application area of metal contacts to silicon carbide.

The book should be of high interest for technologists, scientists, engineers and graduate students who are working in the field of silicon carbide and related materials. The book also can be used as a supplementary textbook for graduate courses on related specialization.

Konstantin Vasilevskiy
Konstantinos Zekentes

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CHAPTER 1

Silicon Carbide Surface Cleaning and Etching

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Abstract

Silicon carbide (SiC) surface cleaning and etching (wet, electrochemical, thermal) are important technological processes in preparation of SiC wafers for crystal growth, defect analysis or device processing. While removal of organic, particulate and metallic contaminants by chemical cleaning is a routine process in research and industrial production, the etching which, in addition to structural defects analysis, can also be used to modify wafer surface structure, is very interesting for development of innovative device concepts. In this book chapter we review SiC chemical cleaning and etching procedures and present perspectives of SiC etching for new device development.

Keywords

Silicon Carbide, Chemical Cleaning, Wet Etching, Electrochemical Etching, Porous SiC

Contents

1. Introduction

Silicon carbide is a semiconductor material which has suitable properties for various electronic applications, mainly in medium- and high-voltage power devices [1,2]. Due to the excellent material characteristics SiC devices can outperform silicon counterparts in terms of blocking voltages and operating temperatures [3]. Electronic products incorporating SiC can be smaller, require less cooling and can operate under harsh conditions which are out of operational window for silicon-based technologies. For example, in hybrid/electrical vehicles, power devices based on SiC allow to improve fuel economy and offer higher flexibility in designing and positioning various system components [4–6]. Semiconductor companies have already introduced SiC based diodes and transistors into the market. However, SiC crystal growth and device processing have not reached similar maturity like silicon technologies. Intensive research and development is still being carried out regarding the single crystal SiC bulk growth process optimization and crystal diameter enlargement as well as on improvement of device processing procedures to reduce fabrication costs and increase device performance [6,7]. While industry is focusing on power technologies, academic research on SiC is shifting towards various innovative device concepts, some of which are discussed in this chapter.

In crystal growth and device processing, a clean SiC substrate surface is crucial in obtaining high yield and reliability. For example, solid particles present on the SiC substrate prior to epitaxial or bulk growth could lead to formation of structural defects which significantly deteriorate crystal quality and material yield. In device processing, improper surface cleanliness could cause numerous problems ranging from impair adhesion of photoresist films to formation of electrical defects in oxide layer. Basic chemical cleaning techniques for SiC were adapted from silicon industry. In contrast to chemical cleaning, wet etching for surface modification or structural defects analysis requires more aggressive process for SiC compared to silicon. In this book chapter, the most common SiC chemical cleaning, wet and thermal etching processes which are applied in research and development, are reviewed. Even though such processes have

been explored for decades, there are still novel findings which could lead to new avenues in research and development. Some applications of wet and thermal etching for innovative SiC device concepts are also presented.

2. Wet chemical cleaning of SiC

2.1 Surface contaminations

Most common contaminants on semiconductor surfaces are organic/molecular films, solid particles, various metals or their ions. In case of SiC, there is also a native oxide layer. It has been shown that silicon dioxide (SiO_2) with a thickness of 1 nm forms on SiC surface in a matter of minutes after chemical cleaning procedures [8,9]. Such oxide should be removed before measurements using surface sensitive techniques or growth of low dimensional materials such as graphene. In general, contaminants can originate from a wide range of sources such as the ambient, wafer dicing, chemicals, personnel etc. Organic compounds, which are present even in a clean-room air, readily adsorb on any semiconductor surface. They can form an organic film and mask some of the particles already residing on the surface. Upon high temperature growth of epitaxial layers or bulk material, organic contaminants carbonize and can form a nucleation point for various structural defects (microcracks, dislocations, stacking faults etc.). Similar defects in crystal growth will occur if solid particles are present on the surface. In device processing, solid particles would affect the entire device fabrication chain by being embedded in deposited films or acting as a mask in photolithographic processes. Metallic contaminants (Fe, Al, Ni, Cu etc.) and ionic metals (Ca, Na) from liquid chemicals, water, metallic tools used to handle SiC sample or measurement equipment could also influence semiconductor device fabrication. For example, commonly used mercury (Hg) probe capacitance-voltage measurement equipment can also leave traces of Hg on the SiC and have to be removed [10]. During heat treatment steps in device fabrication, metallic contaminants can diffuse into the semiconductor and introduce defect levels/traps in the band gap causing device degradation. Due to differences in materials parameters (chemical bond strength, diffusion coefficients, surface energies) of Si and SiC, the latter is less sensitive to diffusion of metallic contamination into bulk material at similar processing temperatures. However, it has been shown that some metallic impurities can degrade intrinsic lifetime of gate oxides [11,12]. Thus their removal and monitoring, for example using the total reflection X-ray fluorescence spectroscopy [13], are important issues in SiC MOSFET fabrication.

2.2 RCA, Piranha and HF cleaning

The most widely used and best-established cleaning solutions for SiC have been transferred from the Si industry. The most common chemistries are the well-known RCA (also called "standard clean" or "SC") and Piranha cleaning. Of course, before applying any of these cleaning procedures the sample can be pre-clean in ultrasonic bath using isopropanol at 80^{o}C followed by rinsing in deionized water.

The RCA process was first introduced in device production at RCA (Radio Corporation of America) in 1965 and its detail description was published by W. Kern and D. D. Puotinen in 1970 [14]. At that time, it was a breakthrough in the semiconductor surface cleaning technologies and it still remains as the most widely used chemical cleaning procedure not only for Si, but for SiC as well. The process is based on a two-step oxidizing and complexing treatment with hydrogen peroxide solutions [15] :

- 1st step or SC1 - cleaning in an alkaline mixture (5 H_20:l H_2O_2(30%):l NH_4OH(29%)). The composition of the solution can vary from 5:1:1 to 7:2:1 parts by volume of H_2O, H_2O_2, and NH_4OH. The treatment is done in ultrasonic bath for 5-10 min at solution temperature of 65-75 ^{o}C followed by rinsing in deionized (DI) water. The SC1 is mainly used for cleaning of organic contaminants which are removed by oxidative breakdown and dissolution. During the treatment the native oxide layer slowly dissolves and a new one is formed by oxidation. Such oxide regeneration process acts as a self-cleaning effect which aids to dislodge particles [16]. The SC1 also removes traces of IB, IIB metals (Au, Ag, Cu, Zn, Cd, Hg) and some other elements like Ni, Co, and Cr by complexing. The SC1 solution possesses poor thermal stability leading to decomposition of H_2O_2 to H_2O and oxygen, and evaporation of NH_3 from NH_4OH. Therefore, a freshly prepared mixture of chemicals has to be used for each cleaning cycle.

- 2nd step or SC2 – cleaning in an acid mixture (6 H_20:1 H_2O_2(30%):1 HCl(27%)) using ultrasonic bath with solution temperature and treatment time similar to SC1. It removes alkali ions, and cations such as $A1^{+3}$, Fe^{+3} and Mg^{+2} as well as metals which were not completely removed during the first step. HCl in SC2 solution is used to increase oxidation strength and complexing of metals [17]. After the SC2 process the sample should be rinsed in DI water. Also, as in SC1, a freshly prepared mixture of chemicals is strongly recommended for each cleaning cycle.

Another strong acid wet cleaning used for SiC is a mixture of 4 H_2SO_4(98%): 1 H_2O_2(30%) so-called "Piranha" clean. The surface is exposed to this mixture for at least 10 min at 100-

130 ^{o}C. The Piranha clean is primarily used for removing the photoresist and heavy organic contaminants. The mixture is extremely dangerous to handle due to its great ability to eradicate organics. The advantage of Piranha over RCA cleaning for organic residues cleaning was demonstrated in SiC biocompatibility studies by S. Saddow et al. [18].

In the original RCA clean process for Si, an optional step of HF cleaning after SC1 can be introduced [14]. The main purpose of this step is to remove oxide film which may form during SC1 step and entrap some trace impurities. However, it was noted that such cleaning will result in recontamination of the Si surface if the HF solution is not of a very high purity and particle-free [16]. In addition, it was not advisable to use HF cleaning after SC2 step since it would cause loss of the protective SiO_2 film that passivates the silicon surface. In case of SiC, the HF treatment is used to remove SiO_2 before surface sensitive measurements or growth of low dimensional materials, such as graphene by sublimation [19], where presence of oxygen is not tolerated. The HF is typically diluted with DI water to slow down the etch rate of SiO_2 and obtain better etching uniformity. The dilution ratios can vary from 1 H_2O:1 HF to 100 H_2O:1 HF [20]. The etching time depends on dilution ratio. For example, the etch rate of SiO_2 with 10 H_2O:1 HF is ~10 Å/s [21,22]. The HF may be diluted with ammonium fluoride (NH_4F). In this case the treatment is called a Buffered Oxide Etch (BOE) or Buffered HF (BHF). Buffered HF is used instead of dilute HF when films, such as photoresist, that could be damaged by a highly acidic environment are present on the wafer surface or when there is a need to remove a large amount of oxide [17].

Numerous studies were performed to analyse wettability of differently processed SiC surfaces after HF cleaning [20,23,24]. King et al. [20] demonstrated that, in addition to chemical treatment, the wettability of SiC depends also on the initial state of the surface (Table 1).

Table 1. Wetting characteristics of as -polished and thermally oxidized 6H-SiC [20].

Treatment	6H-SiC (0001) as-polished	6H-SiC (0001) after oxide removal using HF
None	Hydrophobic	Hydrophilic
SC1	Hydrophilic	Hydrophilic
SC2	Hydrophobic	Hydrophilic
10 H_2O:1 HF	Hydrophobic	Hydrophilic
Piranha	Hydrophilic	Hydrophilic

The same authors showed that the hydrophilic nature of SiC surfaces produced in wet chemical cleaning could lead to trapping of contaminants in micropipes and their removal/outgassing in subsequent processing [25].

Despite the effectiveness of any cleaning technique the semiconductor surface can be contaminated again by improper rinsing, drying or post-cleaning storage. Cleaned glass or stainless-steel containers flushed with high purity nitrogen and stored in a clean room environment could be considered for sample storage [16]. For a longer storage, or transportation of SiC samples, evacuated plastic bags could also be used. Handling samples with metal tweezers would leave traces of metals on the surface. Using vacuum tweezers would at least allow avoiding such contamination on the front side of the sample.

3. Chemical, electrochemical and thermal etching of SiC

3.1 Chemical etching

Silicon carbide is resistant to any chemical solutions at room temperature due to the very high chemical inertness [26]. Therefore, chemical etching of SiC can only be achieved by hot gases or molten salts and alkali solutions at high temperatures. Only etching using molten salts will be discussed in this chapter. The etching mechanism is based on breaking SiC bonds on the surface by reactive molecules from molten salts followed by formation of oxides which are subsequently dissolved in the same solution.

Various studies were dedicated to investigate the effect of different molten salts like $KClO_3$, KCl-NaCl, K_2CO_3, K_2SO_4, KNO_3, $Na_2B_4O_7$, Na_2CO_3, $NaNO_3$, Na_2SO_4, NaF: Na_2SO_4, PbF_2 and other, but in most cases there were problems with chemical attack to the crucible, need for high process temperature or stability of molten salt itself [26–35]. Today, the most common way to reveal structural defects in single crystal SiC wafers by chemical etching is to use molten KOH. A typical KOH etching set-up is made of ceramic heater equipped with thermocouple and nickel crucible. The thermocouple encapsulated in Ni tube can be dipped in molten KOH as close as possible to the sample to obtain more accurate temperature reading [36]. A small basket/holder made of nickel or platinum is used to immerse the SiC sample in molten KOH at 400–600 °C. The etching rates may vary depending on temperature, crystal orientation or etching atmosphere during the KOH etching. A very detailed study on etching rates of SiC in molten KOH has been done by Katsuno et al. [37]. The authors have reported that the etching rate at 520 ^{o}C is about four times higher on $(000\bar{1})$ surface (~2.3 μm/min) compared to (0001) surface (~0.6 μm/min) while etching rates of the $(11\bar{2}0)$ and the $(1\bar{1}00)$ surfaces are almost equal to that of the $(000\bar{1})$. In addition, they demonstrated that for n- and p-type samples the carrier concentration hardly influence the etching rate up to 3×10^{19} cm^{-3} and that the etching rate is enhanced by about 2% as the hexagonality of SiC crystals increases from the 6H(33%) < 15R(40%) < 4H(50%). Mokhov et al.

showed that the etching rate of the neutron-irradiated SiC polar faces in the KOH melt depends on the irradiation dose or density of radiation induced point defects [38].

The primary use of molten KOH is to reveal and analyze various defects on SiC surfaces. Crystal areas containing defects have higher strain energies compared to single crystal areas. Thus, they are more sensitive to chemical attack and this leads to preferential etching [39]. Various defects can be identified based on the shape of the etch pit and information on their densities and interactions can be obtained [40,41]. The most common defects in hexagonal SiC which can be revealed by molten KOH etching, are screw dislocations (SDs), threading edge dislocations (TEDs), basal plane dislocations (BPDs) [36,42–47] (Fig. 1a). Screw dislocations can be divided into closed-core (threading screw dislocations (TSDs)) and hollow-core (micropipes (MPs)) dislocations. The hollow cores become evident when the Burger vector exceeds lattice parameter at least two times in 6H SiC and three times in 4H-SiC [48,49]. Stacking faults occurring as linear etch pits after etching can be delineated on the cleavage of $(11\bar{2}0)$ and $(1\bar{1}00)$ planes [50–54]. Typical imaging and counting of defects can be performed using an optical microscope with Nomarski Differential Interface Contrast (NDIC). Sakwe et al. pointed out the importance of KOH etching process optimization in order to avoid over etching and merging of different etch pits [36]. There is a difference in etching selectivity on the (0001) and the $(000\bar{1})$ faces. Syväjärvi et al. showed that (0001) is etched preferentially, whereas the $(000\bar{1})$ is etched nearly isotropically [55]. Such anisotropy is clearly seen when comparing micropipe-related pit diameter on etching time on both polar faces of SiC (Fig. 1b). The openings related to micropipes are at least a factor of 10 smaller on the $(000\bar{1})$ face and they possess roundish shape instead of hexagonal on the (0001) face [55,56]. The shape of the etch pit can be greatly influenced by the conductivity and doping concentration. For example, the p-type (0001) face in 4H-SiC possesses much stronger preferential etching compared to n^+ samples, on which mainly round pits with continuous size distribution is formed [44]. The authors attributed this difference to band bending structure and injection of holes at the 4H-SiC/KOH interface depending on the conductivity type. Based on their theory, in the case of molten KOH etching of highly n-type 4H-SiC, electrochemical processes become dominant due to formation of a p-type inversion layer on the SiC surface and this is resulting in isotropic etching. Such dependence of molten KOH etching on doping made it very difficult to distinguish etch pits of TSDs and TEDs in heavily ($n>6\times10^{18}$ cm^{-3}) n-type doped SiC [44,60,61]. Nevertheless, it was shown that TSDs (or TEDs) can be identified with very high accuracy after etching in molten KOH:Na_2O_2=50:3 [61]. Another report showed that the etch pit size of TSDs and TEDs in highly n-type 4H-SiC differs more greatly when more than 20-wt.% Na_2O_2 is added to the KOH [62]. The authors claimed that such

improvement was achieved due to dissolved oxygen which enhanced the defect-selective anisotropic etching. Cui et al reported that combination of molten KOH etching with laser confocal microscopy can also be a powerful tool to identify and characterize TEDs and TSDs in n-type and semi-insulating SiC wafers based on etch pit sectional view information and etch pit angle [38].

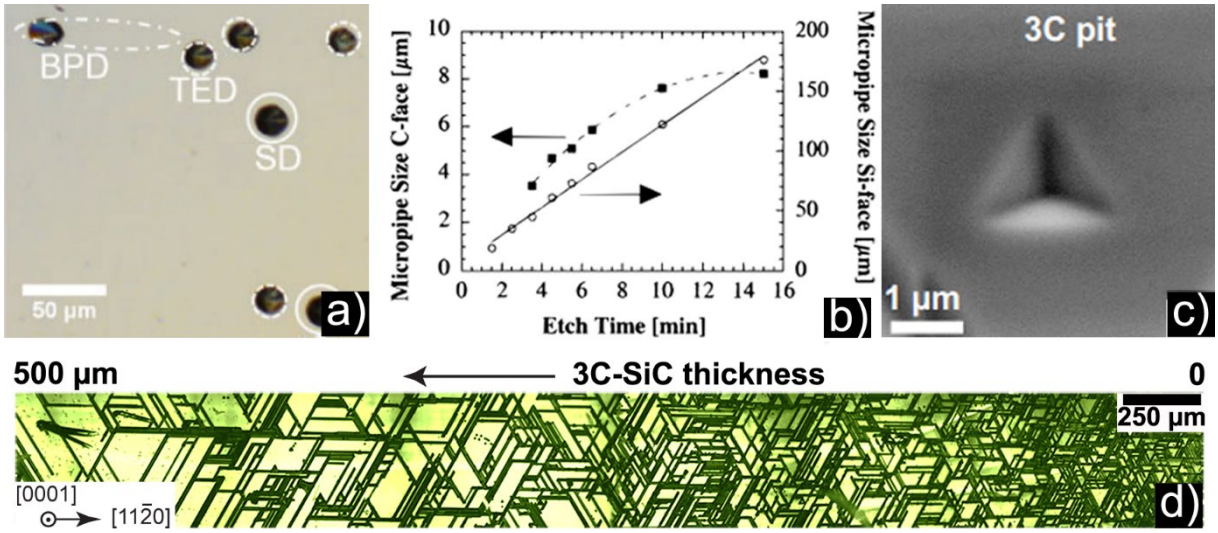

Figure 1. a) etch pits in 4H-SiC (0001) [57] *(Copyright 2014 The Japan Society of Applied Physics),*
b) micropipe related pit diameter vs. etching time for Si- and C-faces [55] *(Reproduced with permission from J. Electrochem. Soc., 147, 3519 (2000). Copyright 2000, The Electrochemical Society.),*
c) etch pit in 3C-SiC(111) after etching in molten KOH [58] *(P.G. Neudeck, A.J. Trunek, D.J. Spry, J.A. Powell, H. Du, M. Skowronski, X.R. Huang, M. Dudley, CVD Growth of 3C-SiC on 4H/6H Mesas, Chem. Vap. Depos. 2006, 12, 531–540. Copyright Wiley-VCH Verlag GmbH & Co. KGaA. Reproduced with permission.),*
d) stacking faults density vs thickness in 3C-SiC(111) revealed by etching in KOH [59] *(Reprinted with permission from Cryst. Growth & Des. 15, 2940-2947 © (2015) American Chemical Society).*

Defects which can be revealed by KOH etching in cubic SiC are stacking faults (SFs), double positioning boundaries (DPBs) and threading edge dislocations (TEDs). Triangular etch pit (Fig. 1c) is a characteristic feature of threading screw dislocations in (111) crystals [39]. Stacking faults density variation with the thickness can be analyzed in 3C-SiC (111) grown on off-oriented hexagonal SiC substrates (Fig. 1d) [59].

3.2 Electrochemical etching

Unlike chemical etching described in Section 3.1 the electrochemical etching can be done at room temperature. In the electrochemical etching cell, the SiC sample and a counter electrode are immersed in electrolyte. By applying an external voltage between them, one can regulate the electric field in the space charge region to inject holes at the interface with the electrolyte what causes oxidation and dissolution of SiC material.

In case of p-type material, the etching process can occur in darkness while etching of n-type material needs UV illumination to generate minority carriers [63]. The most common electrolytes used in electrochemical etching are fluoride or alkaline based solutions: HF, KOH, NaOH, H_2SO_4, HCl, and H_2O_2 [27]. The vast majority of studies in electrochemical etching of SiC have been done using HF. It has been suggested that the following reactions occur during the electrochemical etching of SiC in HF solutions [64,65]:

$$SiC+4H_2O+8h^+ \rightarrow SiO_2+CO_2+8H^+ \quad (1)$$

$$SiC+2H_2O+4h^+ \rightarrow SiO+CO+4H^+ \quad (2)$$

$$SiO_2+HF \rightarrow H_2SiF_6+2H_2O \quad (3)$$

The first two equations describe electrochemical oxidation while the third equation shows dissolution of oxide in HF solution. Electrochemical etching of SiC leads to formation of porous structure. There are always nanometer size fibers left behind as the etching front moves into the bulk material. The protection of porous structures from being completely etched away as the porosity increases was explained by formation of space charge region at the SiC/electrolyte interface [66,67]. The morphology of the etched SiC depends on polarity [68,69], current density [70] and electrolyte solution [71]. It has been shown that n-type heavily doped 4H-SiC wafers can be electrochemically anodized in a HF-based electrolyte without any UV light assistance [68]. The authors used HF mixed with acetic acid (to increase electrolyte wettability) and water with volume ratios HF(50%):acetic acid:H_2O of 4.6:2.1:1.5. Usually a dendritic porous structure is formed on (0001) face while $(000\bar{1})$ face leads to columnar structure [68,69]. Also, it was reported that a thin skin layer on top of the porous structure can form inducing an inhomogeneous pattern of the pores [69,72]. Inhomogeneities in pore structures were obtained by applying constant current or constant voltage conditions [67,73]. In contrast, porous 4H-SiC with tailored properties can be prepared by combining metal assisted photochemical etching (MAPCE) and photoelectrochemical etching (PECE) steps [74–76]. A noble metal is deposited on SiC surface in MAPCE process. The sample is then immersed in HF solution containing

oxidizing agent. The deposited metal acts as local cathode where the oxidizing agent is reduced, and the surface areas not covered with the metal get porosified. A porous layer generated with MAPCE provides initiation sites for PECE, thus the formation of a skin layer can be avoided.

3.3 Thermal etching

Various SiC surface contaminants can be removed using chemical cleaning procedures such as those described in section 3.1. However, removal of surface scratches remaining after mechanical polishing or modification of surface steps structure require more reactive surface treatment such as hydrogen etching or chemo-mechanical polishing (CMP). Hydrogen etching is performed *in situ* in the CVD reactor using fluxes of H_2+HCl, H_2+C_3H_8 or H_2+SiH_4 gases at temperatures of 1300-1600 ^oC [77,78]. In addition to removal of surface scratches, it is possible to control surface step morphology, but it is quite an expensive process. The CMP combines mechanical polishing and chemical etching simultaneously using special slurries [79–81], thus very smooth surfaces can be obtained. However, surface structure engineering is not possible, since the CMP is suitable only for surface planarization. An alternative technique, which does not require any aqueous solutions or dangerous gases, is thermal etching. Originally it has been used to pre-etch SiC seeds by reversing temperature gradient during sublimation growth of bulk SiC crystals [82]. Since the quality of the SiC seeds has significantly improved since 90s, the thermal etching is mainly used for SiC surface step engineering. Thermal etching of SiC is based on sublimation decomposition of SiC at elevated temperatures [83–87]. The etching of SiC surface is usually performed in a graphite crucible. Upon sublimation the SiC surface decomposes with the highest partial vapor pressure of Si followed by SiC_2 and Si_2C [88]. The composition of vapor species above the SiC crystal depends on temperature and it has been calculated that the atomic flow of C is less than 1% of the atomic flow of silicon in the Si-C chemical system [88]. Therefore, if loss of Si is not compensated and accumulation of C on the surface is not prevented, there is graphitization of SiC surface upon high temperature annealing. It has been demonstrated that graphitization can be significantly suppressed by placing Ta near the SiC surface [89]. In the Si-C-Ta material system Ta reacts with the carbon containing vapor species by forming stable carbide. Therefore, in the etching cavity with Ta, the following reaction is thought to occur:

$$Ta\ (solid) + Si_2C(gas) \rightarrow TaC(solid) + 2Si(gas) \quad (4)$$

This implies that Ta creates more Si-rich environment, Si reacts with carbon bearing species and provides conditions for thermal etching of SiC surface. Lebedev et al. demonstrated that atomically flat 6H-SiC (0001) surface with terraces separated by steps of unit-cell height (h = 1.5 nm) can be obtained on mechanically polished 6H-SiC (0001) after etching in vacuum (~10^{-6} mbar) at 1300-1400 °C [83]. Nishiguchi et al. investigated effect of nitrogen and argon ambient to the etching of $(11\bar{2}0)$, $(000\bar{1})$ and (0001) surfaces of 6H-SiC at 2500 ^{o}C [84]. They found that etching in nitrogen atmosphere provides better surface morphology compared to argon. In addition, step bunching was a serious problem in obtaining flat surfaces on 6H-SiC (0001) substrates, but it hardly occurred on the $(11\bar{2}0)$ substrates and atomically flat surface was obtained (Fig. 2a-f). Jokubavicius et al. performed thermal etching experiments of 6H-SiC (0001), 4H-SiC (0001) and 3C-SiC (111) surfaces in argon (700 mbar) and vacuum (~10^{-5} mbar) at isothermal conditions (Fig. 2g) [87]. They observed that after thermal etching the smoothest surfaces can be obtained in 3C-SiC(111) and attributed that to differences in step bunching formation in hexagonal and cubic polytypes. All SiC polytypes are composed of SiC bilayers which are stacked on top of each other. The energies of interaction between each SiC bilayer plane vary depending on unique stacking sequence of specific polytype. This induces variations in step dynamics and formation of step bunching upon crystal growth or sublimation/thermal etching. The 3C-SiC is the only polytype in which the interaction energy between different SiC bilayer planes is the same, thus energetically driven step bunching is not expected [90,91].

4. Perspectives of SiC etching for various device concepts

4.1 Fluorescent SiC for white LEDs

In most cases, wet chemical etching is used to fabricate porous structure on single crystal SiC surface. Considering small size of the pores one can expect quantum size effects to occur upon light illumination and this is primarily interesting for optoelectronic applications. Matsumoto et al. showed that blue-green emission from n-type 6H-SiC can be tuned by porous structure electrochemically etched in HF-ethanol solution [92]. The blue shift in the electroluminescence of n-type 6H-SiC with porous structure etched in HF solution illuminated with UV light was demonstrated by Rittenhouse et al. [93]. The properties of porous structures have been realized to be very useful in white light emission diode (LED) based on fluorescent SiC layer which converts UV to visible light. The initial idea of such white LED concept based on fluorescent SiC was proposed by Kamiyama et al. [94,95]. The proposed structure of the device contained donor and acceptor doped SiC as a phosphor material, called fluorescent SiC, which is excited by

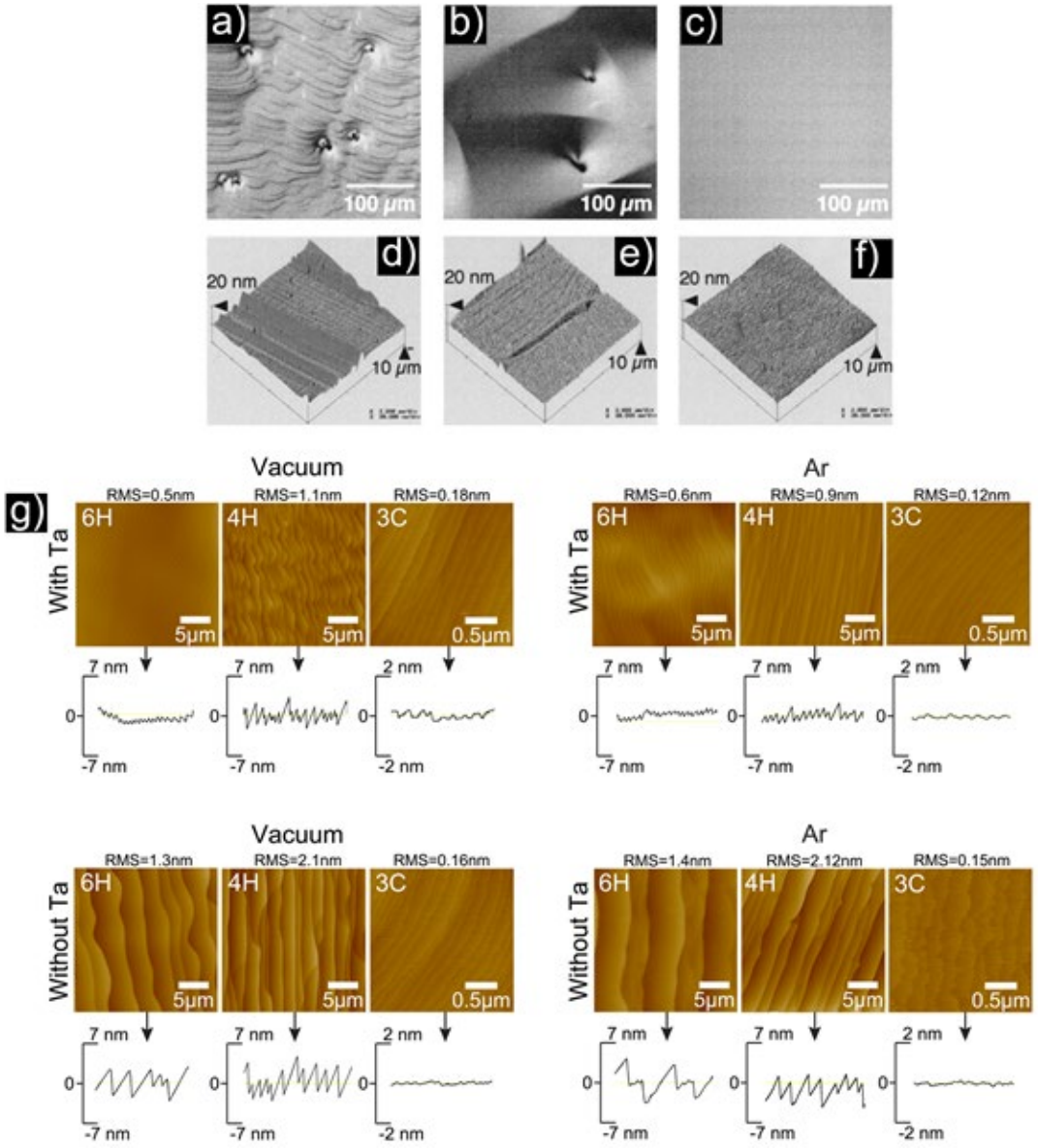

Figure 2. Optical images (a, b, c) and AFM images (d,e,f) of 6H-SiC substrates after thermal etching at T=2500 ^{o}C and p=700 Torr in nitrogen atmosphere for 30 min. (a and d) Si-face, (b and e) C-face, (c and f) (11$\bar{2}$0) surface (Copyright 2003 The Japan Society of Applied Physics) [84]. g) AFM images of 6H-, 4H-SiC (0001) and 3C-SiC(111) after etching for 10 min at 1800^{o}C using different arrangements and ambient conditions[87] (Reprinted with permission from V. Jokubavicius, G.R. Yazdi, I.G. Ivanov, Y. Niu, A. Zakharov, T. Iakimov, M. Syväjärvi, R. Yakimova, Surface engineering of SiC via sublimation etching, Appl. Surf. Sci. 390 (2016) 816. Copyright (2016) Elsevier B.V.).

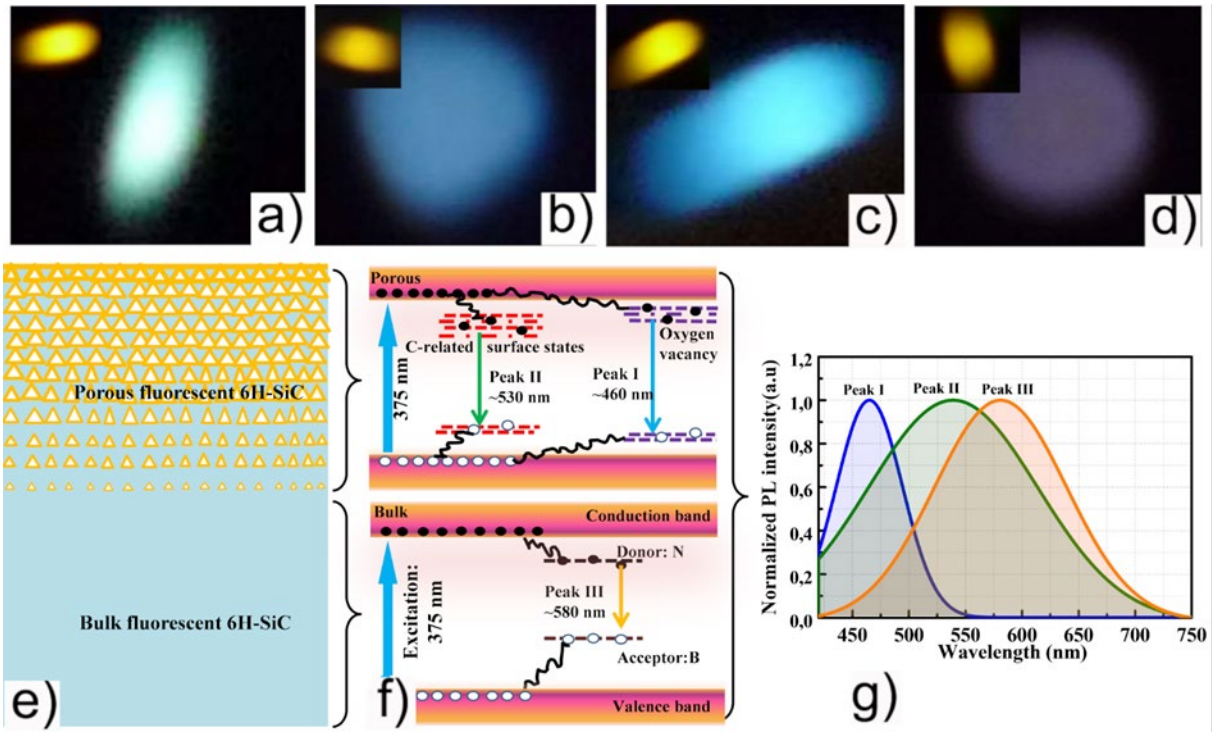

Figure 3. PL images of porous fluorescent SiC fabricated by electrochemical etching in a) diluted HF, emission peak at 491 nm b) diluted HF+$K_2S_2O_8$ (0.01 mol), emission peak at 449 nm, c) diluted HF+ $K_2S_2O_8$ (0.015 mol), emission peak at 434 nm, d) diluted HF+ $K_2S_2O_8$ (0.02 mol), emission peak at 407nm. Yellow insets in a-d correspond to emission from N-B doped 6H-SiC at about 580 nm [96] *(T. Nishimura, K. Miyoshi, F. Teramae, M. Iwaya, S. Kamiyama, H. Amano, I. Akasaki, High efficiency violet to blue light emission in porous SiC produced by anodic method, Phys. Status Solidi. 7 (2010) 2459–2462. Copyright Wiley-VCH Verlag GmbH & Co. KGaA. Reproduced with permission.), e) schematic diagram of the fluorescent 6H-SiC with porous surface layer, f) three possible transitions related to: I) surface defects in porous SiC, II) oxygen vacancy, III) DAP recombination in N-B doped 6H-SiC, g) emission spectra from porous SiC layer* [97].

UV light produced by nitride LEDs grown on doped SiC. Donor and acceptor pairs (DAPs) of N-B and N-Al in 6H-SiC layers can cover almost the entire visible spectral range. Such fluorescent SiC would possess uniform and stable color quality and an excellent thermal conductivity for high-power-operated LEDs. Moreover, SiC is well established substrate for nitride growth, thus a monolithic LED structure containing nitrides and fluorescent SiC is possible to fabricate. However, the emission efficiency of N-Al DAPs is much lower than that of N-B DAPs due to much higher thermal ionization

for shallower Al-acceptor states. Therefore, the emission from N-Al should be obtained by other means. Nishimura et al demonstrated that this could be done by etching porous structure on N-B doped SiC [96]. To control the porosity of N-B doped SiC they used electrochemical etching in HF diluted with $K_2S_2O_8$. This gives effect on light emission as shown in Fig. 3a-d. The latter study was expanded by Lu et al who introduced a passivation layer of Al_2O_3 on porous structure to significantly enhance the emission of light (Fig. 3e-g) [97]. Moreover, the authors demonstrated that porous layers fabricated in commercial n-type and lab grown N-B co-doped 6H-SiC show emission peaks centered approximately at 460 nm and 530 nm. Those peaks were attributed to neutral oxygen vacancies and C-related surface defects generated during anodic oxidation process. The B-N DAP emission peak in 6H-SiC is usually positioned at about 580 nm. As shown in Fig. 3g, all three peaks can cover very broad visible light spectrum.

4.2 Rugate mirrors

As the porosity of etched SiC layer increases and structural inhomogeneities become smaller than typical wavelengths, the porous layer possesses refractive index *n* which depends on the structure. Higher porosity typically leads to a lower refractive index since the dielectric effective medium contains more air. Such engineering of optical properties in porous SiC can be used to fabricate rugate mirrors. The advantage of SiC based rugate mirrors is the possibility to use them in high temperature and chemically aggressive environment which is too hostile for other materials. As mentioned in section 3.2 of this book chapter, the conventional electrochemical etching of SiC can lead to formation of a skin layer on top of the porous structure or an inhomogeneous pattern of the pores. These problem can be solved by combining metal assisted photochemical etching (MAPCE) and photoelectrochemical etching (PECE) steps [74,75].

The fabrication of rugate mirror is divided in three steps:

1) To avoid skin and cap layer formation a porous SiC layer with the thickness of about 1 μm is formed by MAPCE.
2) PECE with etching solution (0.04M $Na_2S_2O_8$ in 1.31 mol/l HF) exposed to UV light is used to fabricated SiC layer with uniform porosity with the thickness of about 30 μm by varying the voltage as a function of transferred charge [98].
3) By applying two 60 V pulses, each lasting 6 s, at the end of the etching process the porous layer is separated from the bulk material which can be re-used for another mirror fabrication (Fig. 4b).